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ML7105 Hardware Design Manual

Bluetooth® Low Energy

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Preface

This hardware design manual describes how to use the board and peripheral devices of ML7105, a 2.4 GHz-band radio communication LSI conforming to Bluetooth® Low Energy.

The following related manuals are available and should be referenced as needed:

- ML7105-XXX Datasheet
- Bluetooth Application Controller Interface (BACI) Command Manual
- Application Developer's Guide for ML7105
- ML7105 User's Manual

Notation

Classification	Notation	Description
● Numeric value	0x*nn*	Represents a hexadecimal number.
	0b*nnnn*	Represents a binary number.
● Address	0x*nnnn_nnnn*	Represents a hexadecimal number. (Indicates 0xnnnnnnnn)
● Unit	word, W	1 word = 32 bits
	byte, B	1 byte = 8 bits
	Mega, M	10^6
	Kilo, K (uppercase)	2^{10}=1024
	Kilo, k (lowercase)	10^3=1000
	Milli, m	10^{-3}
	Micro,μ	10^{-6}
	Nano, n	10^{-9}
	Second, s (lowercase)	Second
● Term	"H" level	Signal level on the high voltage side; indicates the voltage level of V_{IH} and V_{OH} as defined in electrical characteristics.
	"L" level	Signal level on the low voltage side; indicates the voltage level of V_{IL} and V_{OL} as defined in electrical characteristics.

● Register description
Read/write attribute: R indicates read-enabled; W indicates write-enabled.
MSB: Most significant bit in an 8-bit register (memory)
LSB: Least significant bit in an 8-bit register (memory)

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1. Using Bypass Capacitors

The figure below shows the power supply system diagram of ML7105.

•ML7105 Power Supply System Diagram

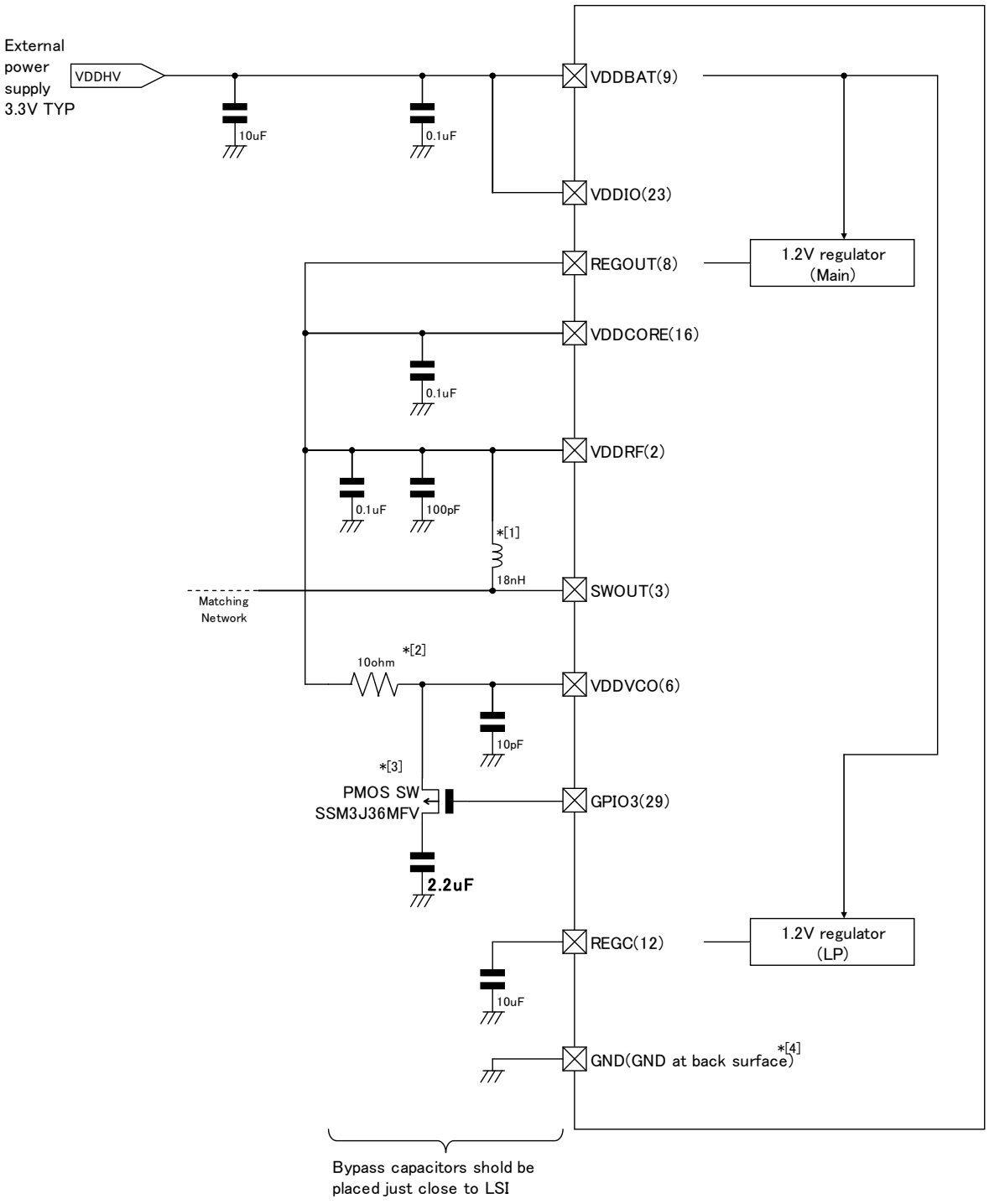


Figure 1.1 ML7105 Power Supply System Diagram

[*1] To supply power to the power amplifier in the LSI, it is necessary to apply DC voltage to the SWOUT(3) pin via an RF choke (inductor).
[*2] As any power supply noise at the VDDVCO(6) pin will degrade the PLL output signal quality, a filter is inserted.
[*3] A PMOS SW is connected to the bypass capacitor 2.2 µF of the VDDVCO(6) pin and controlled by the GPIO3(29) pin. This prevents the electrical charge accumulated in the capacitor from being discharged and reduces the current consumption. The GPIO3(29) pin operates in accordance with the operation mode and connects/disconnects the capacitor according to the ON/OFF state of the 1.2 V regulator to reduce the activation time.
[*4] In the LSI, the analog GNDs and digital GNDs are connected to the GND at back surface.

Note the followings when placing bypass capacitors:

1. The VDD and GND traces should be wider than the other signal line traces to reduce the trace resistance.
2. Bypass capacitors should be placed just close to LSI pins.
3. A bypass capacitor with smaller capacitance needs to be placed more close to an LSI pin.
4. Input/output pins should have a capacitance of about 10 µF to ensure the stability of the 1.2 V regulator (LP).
5. For the VDDBAT(9)/VDDIO(23) pins, LAPIS recommends a 10 µF tantalum capacitor connected in parallel with a 0.1 µF laminated ceramic capacitor. When you connect the VDDBAT(9) pin to the VDDIO(23) pin, the total capacitance should be designed to be about 10 µF.
6. The total capacitance connected to the REGOUT(8) pin should be 0.3 µF or less. If a capacitance of µF order is connected, the current consumption may increase and the activation time may become longer to charge the capacitance. In that case, use MOS_SW as for the VDDVCO(6) pin to prevent the electrical charge from being discharged.
7. In general, ceramic capacitors have specific temperature and voltage characteristics. Select the best capacitor for the operating voltage and temperature of your specific application. If you use high-dielectric capacitors (class II), LAPIS recommends B characteristics.
8. This LSI has the low power consumption mode (Deep Sleep state). In this mode, the current consumption of the LSI is about 0.7 µA and the leakage current from the external capacitor cannot be ignored. To achieve the design with low power consumption, LAPIS recommends to select parts with very low leakage current, considering the leakage current from the used capacitor.

2. Crystal Oscillator Circuit (26-MHz Master Clock)

The figure below shows a configuration example when a crystal oscillator is used. Capacitors for the XOP(13) and XON(14) pins are required so that the crystal oscillator circuit provides stable oscillation of 26 MHz. To determine the constants, LAPIS recommends evaluating the overall capacitance of the board to be used, including the parasitic capacitance.
The considerations should include excitation level, oscillation margin ratio, frequency deviation, and activation time of oscillator circuit.

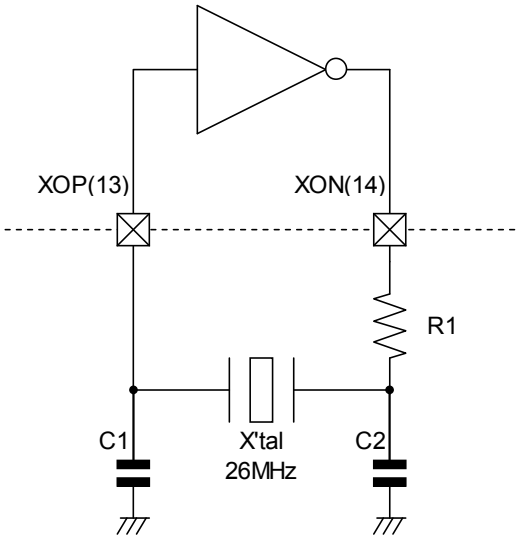


Figure 2.1 Example of ML7105 26-MHz Crystal Oscillator Circuit Configuration

2.1 Circuit Constant on External Board (as Reference Value)

LAPIS recommends to ask your crystal oscillator manufacturer to get the matching property data for your board.
The matching constants for our evaluation board are shown below.

Table 2.1.1 Matching Constants When Using Crystal Oscillator by Seiko Epson Corp.

Oscillator model name	Frequency (MHz)	Equivalent series resistance max (Ω)	Load capacitance (pF)	Constant (as reference value)			Operating condition	
				R1(Ω)	C1(pF)	C2(pF)	Power supply voltage range VDDBAT (V)	Temperature range (°C)
FA20H	26.00	60	8.0	0	10	10	1.6 to 3.6	-20 to 70

Oscillator model name	Frequency (MHz)	Equivalent series resistance max (Ω)	Load capacitance (pF)	Constant (as reference value)			Operating condition	
				R1(Ω)	C1(pF)	C2(pF)	Power supply voltage range VDDBAT (V)	Temperature range (°C)
FA-128	26.00	60	8.0	0	7	8	1.6 to 3.6	-20 to 70

Table 2.1.2 Matching Constants When Using Crystal Oscillator by Daishinku Corp.

Oscillator model name	Frequency (MHz)	Equivalent series resistance max (Ω)	Load capacitance (pF)	Constant (as reference value)			Operating condition	
				R1(Ω)	C1(pF)	C2(pF)	Power supply voltage range VDDBAT (V)	Temperature range (°C)
DSX221G	26.00	60	8.0	0	10	12	1.6 to 3.6	-20 to 70

Table 2.1.3 Matching Constants When Using Crystal Oscillator by Nihon Dempa Kogyo Co., Ltd.

Oscillator model name	Frequency (MHz)	Equivalent series resistance max ( )	Load capacitance (pF)	Constant (as reference value)			Operating condition	
				R1(Ω)	C1(pF)	C2(pF)	Power supply voltage range VDDBAT (V)	Temperature range (°C)
NX2520SA	26.00	60	6.0	0	5	6	1.6 to 3.6	-20 to 70

[Note]
The above circuit constants are values evaluated on a specific sample and board and provided for your information, and thus its content is not guaranteed.

2.2 Notes on Configuring a Crystal Oscillator Circuit

Note the followings when configuring a crystal oscillator circuit:

1. Be sure to set the values of the peripherals (C1, C2, and R1) according to the specifications of the crystal oscillator to be used.
2. Place the peripherals (C1, C2, and R1) just close to the XOP(13) and XON(14) pins to reduce the parasitic capacitance of the board for stable oscillation operation.
3. For the 26-MHz master clock, ensure accuracy[*1] under the recommended operating conditions described in the specifications including temperature variations, power supply voltage variations, and aging changes.
4. Be sure the crystal oscillator circuit does not cross other signal lines.
5. Do not wire signal lines that flow large currents near the circuit.
6. For the oscillator circuit capacitors, make sure the potential of the ground points is always equal to that of the GND. Do not connect the capacitors to GNDs where large currents flow.
7. Do not take oscillation signals from the oscillator circuit.

[*1] When the above accuracy is not satisfied, fine tuning can be performed by using the XO oscillation frequency adjustment function described in section 2.3.

2.3 Frequency Adjustment Using XO Oscillation Frequency Adjustment Function

26 MHz of the master clock can be fine tuned by the XO oscillation frequency adjustment function using the RF registers described below. The RF registers can be read or written by using the BACI Commands or HCI Vendor Commands.
<BACI Command>

- Write_RF_Reg
- Read_RF_Reg

<HCI Vendor Command>

- HCI_VENDOR_RF_RADIO_REG_WRITE
- HCI_VENDOR_RF_RADIO_REG_READ

2.3.1 RF Resistor 23 (XOTRIM2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RF Register23	-*	-*	XO_FFIN						-*	-*	-*	-*	-*	-*	-*	-*
Initial Value	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x17 Initial Value: 0x0800
[Note]*: Do not change the initial value.

[Description of Bits]

Field	bit	Description
XO_FFIN	13:8	Fine-tunes the XO oscillation frequency. 00h: Highest frequency setting (fast), 3Fh: Lowest frequency setting (slow)

Adjustment example:
Step1 Set the 2440-MHz continuous Tx operation state[*1].
Step2 Measure the RF transmit frequency with a frequency counter or spectrum analyzer.
Step3 Use RF Resistor 23 described above to adjust the RF transmit frequency so that its value is within the recommended operating range described in the specifications.

[*1] For setting the continuous Tx operation state, refer to the section "Continuous transmission test" in "7. RF Test Mode & Direct Test Mode" of the "ML7105 User's Manual".

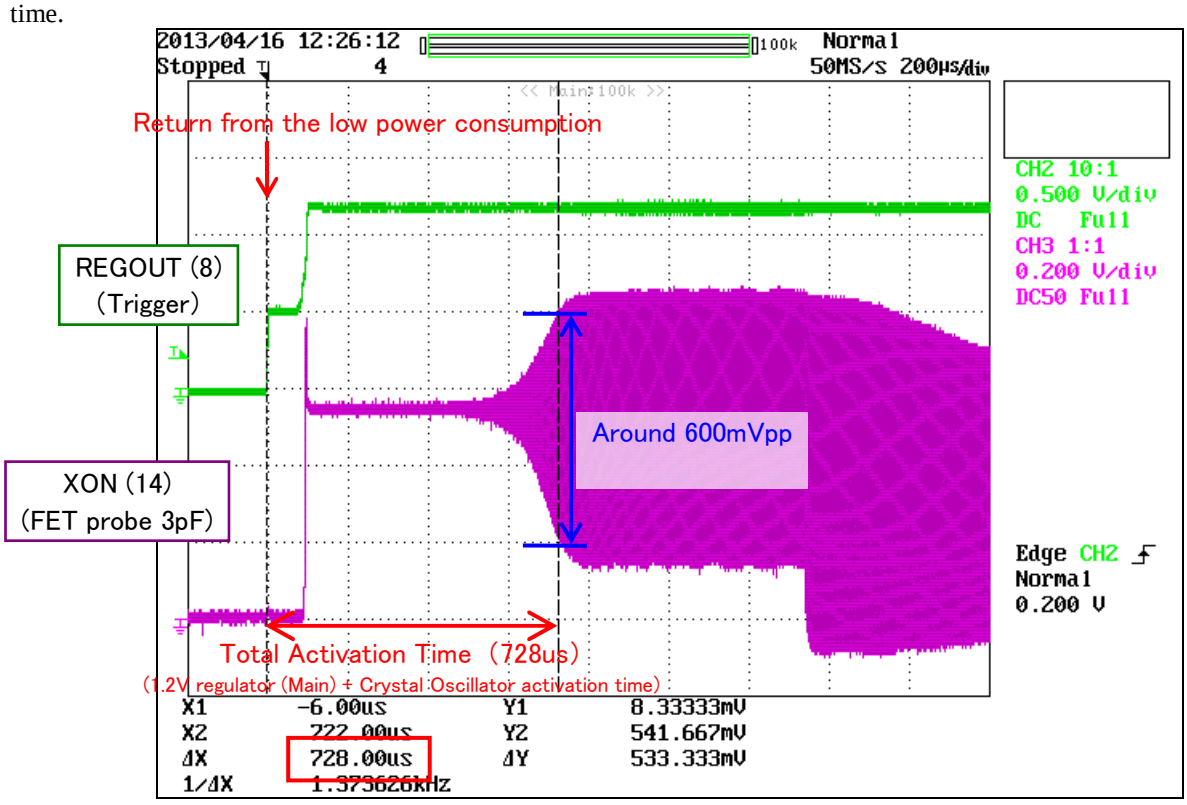
The value of RF Resistor 23 is reset to the initial value (0x0800) each time ML7105 is reset. If you have adjusted the XO oscillation frequency by using the XO oscillation frequency adjustment function, make sure the adjustment value is written to RF Resistor 23 at each reset.

2.4 Activation time of a Crystal Oscillator Circuit

This LSI has the low power consumption mode (Deep Sleep state). In this mode, 1.2 V regulator (Main) and 26MHz Crystal Oscillator Circuit shut down. Make the 26MHz Crystal Oscillator activation time less than 1ms at the time of return from the low power consumption. If the activation time is long, ML7105 can't keep the communication state for the communication timing mismatching.
To determine the constants, LAPIS recommends evaluating the activation time including the parasitic capacitance.

The method of evaluating the activation time:
Step1 Monitor the REGOUT(8) and XON(14) pins with oscilloscope. At monitoring the XON(14) pin, use such as FET probe for decrease the probe parasitic capacitance.
Step2 The voltage of the REGOUT(8) pin rise at the same time of return from the low power consumption. Measure the time till the amplitude of XON(14) pin become around 600mVpp from the voltage of REGOUT(8) pin rise.

The activation time for our evaluation board are shown below. (Using FA20H)
The activation time contains 1.2 V regulator (Main) activation and Crystal Oscillator activation. The target activation time of 1.2 V regulator (Main) is 200us Max. And Crystal Oscillator is 800us Max. Make less than 1ms for the total activation time.



[Note]
The above circuit constants are values evaluated on a specific sample and board and provided for your information, and thus its content is not guaranteed.

3. 32.768-kHz Low Power Clock

ML7105 has the external input mode for the Low power clock.

The figure below shows a circuit configuration example when using the external input mode. When using the external input mode, input a clock which satisfies the following characteristics from the LPCLKIN(11) pin:

- Frequency: 32.768kHz ±250ppm
- Input voltage VIH: 1 to VDDIO[V], VIL: 0 to 0.3[V]
- Duty: 50% ±20%

To use the external input mode, Tx and Rx characteristics may be influenced by the clock. LAPIS recommends to put in damping resistor at LPCLKIN(11) pin when .using the external input mode.
To determine the resistor constant, LAPIS recommends evaluating the Tx and Rx characteristics.

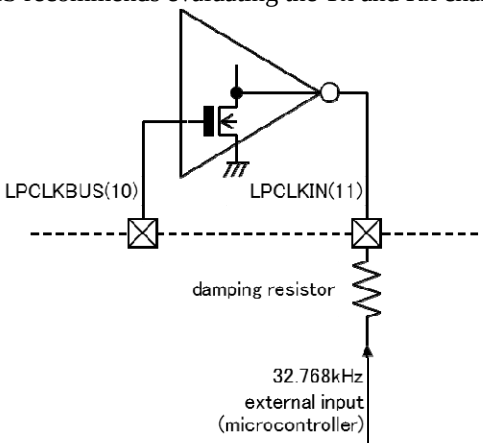


Figure 3.1 Example of ML7105 Circuit Configuration in 32.768-kHz External Input Mode

4. PLL Loop Filter Constant

The figure below shows the PLL loop filter circuit. Use the constants for parts shown in the figure below to achieve good phase noise characteristics. Select parts with good temperature characteristics.

Place the loop filter parts (C1, R1 and C2) just close to the PLLLPF(7) pin to avoid noise contamination. Do not place traces causing noise such as reference clock traces around this pin.

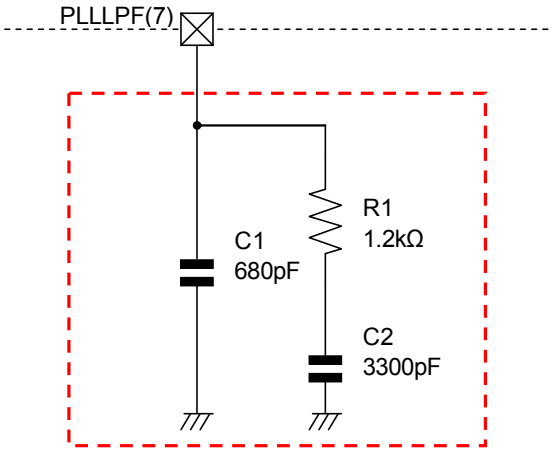


Figure 4.1 ML7105 PLL Loop Filter Configuration

5. RF Matching Constant Design

The figure below shows a standard RF matching circuit configuration.
The REGOUT(8) pin outputs 1.2 V. For PA power supply, the output from the REGOUT(8) pin is applied to the SWOUT(3) pin via the choke coil L1. L3 and C12 constitute a double wave trap. C13 is a capacitor for decoupling. For the VDDRF(2) pin, place 0.1µF and 100pF as bypass capacitors just close to the LSI.

C9 and C10 are used when the matching needs to be changed between RX and TX. The SWRX(4) pin (during Rx) or the SWTX(5) pin (during Tx) is connected to GND by using the SW within the LSI. With the matching of our evaluation board, these are NM (No Mount).

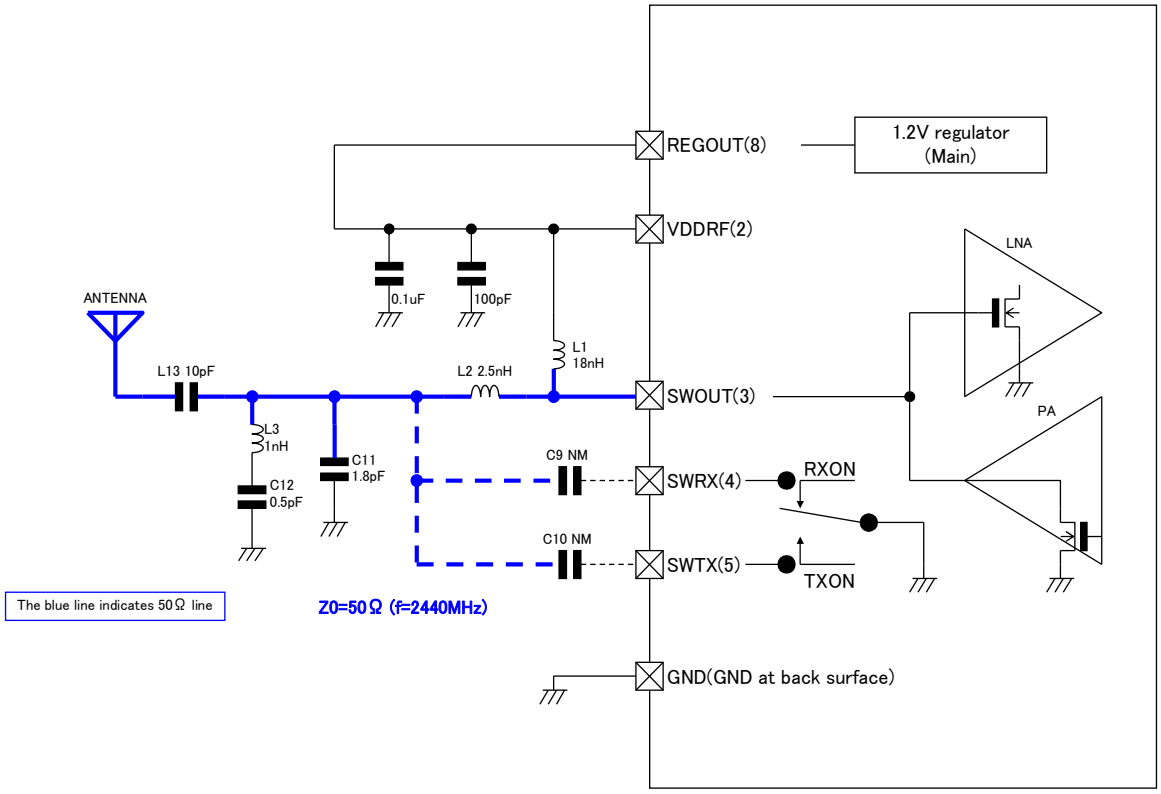


Figure 5.1 Example of ML7105 RF Matching Circuit Configuration

In the above circuit diagram, the matching is adjusted by adjusting L2 and C11. The matching is performed so that the input impedance from the antenna is near 50Ω and VSWR is 2 or less during a continuous Rx operation [*1]. The frequency band to be adjusted is 2402 to 2480 MHz. At this time, if C11 is too large, PA becomes inefficient. Adjust C11 using 2 pF or less as a guide.
After the adjustment, perform a transmission test to make sure that the transmitter power is not reduced.

[*1] For setting the continuous Rx operation state, refer to the section "Continuous reception test" in "7. RF Test Mode & Direct Test Mode" of the "ML7105 User's Manual".

The figure below shows the input impedance characteristics (S11) during a continuous Rx operation of our evaluation board.

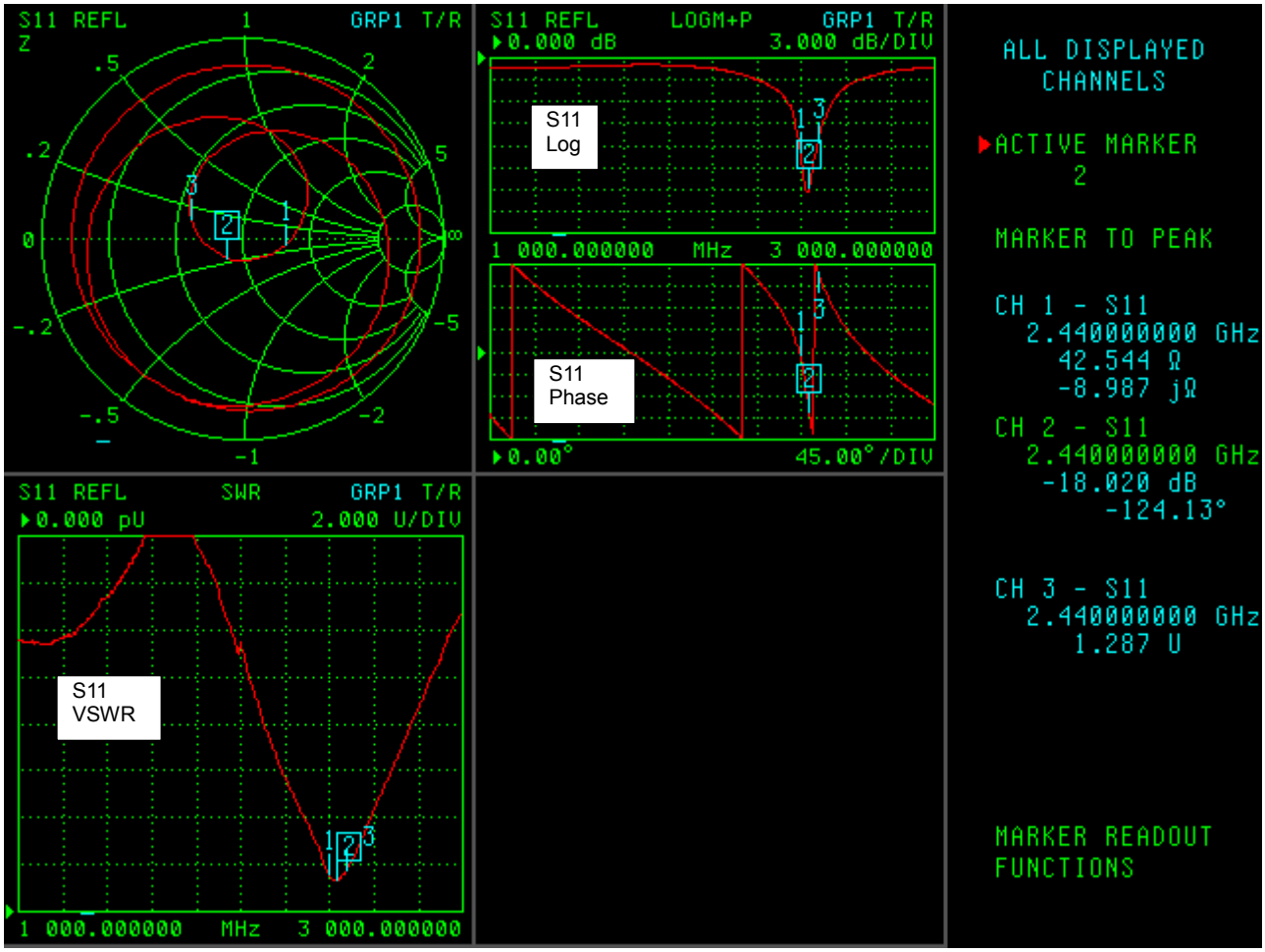


Figure 5.2 ML7105 RF Input Impedance Characteristics (During Continuous Rx Operation)
2402MHz[1], 2440MHz[2], 2480MHz[3]

[Note]
The above measurement result is a value measured for a specific sample and provided for your information, and thus its content is not guaranteed.

6. Selection of Parts

1. Antenna
   LAPIS recommends using an antenna with the specifications shown in Table 6.1.
   Select an antenna with the best directivity characteristics for your specific operating, environmental and installation conditions. Since antennas are affected by installation conditions such as GND, external factors should always be taken into account.
   LAPIS recommends consulting the manufacturer of the selected antenna for installation details in relation to various factors, including the shape and stray capacitance of the board to be used.

Table 6.1 Antenna

Frequency band	2.4-GHz band
In-band VSWR	2.0MAX
Nominal impedance	50Ω

2. External regulator
   Use a regulator that is characterized by high accuracy, low noise, and high ripple elimination and whose operating temperature is appropriate for your purpose.
   If the traces to the power supply input pins and GND pins have too high impedances, the resulting noise will cause return currents that make operations unstable. Therefore, provide sufficiently low impedances for these traces.

3. Inductors
   Use high Q inductors. LAPIS recommends LQW15A series by Murata Manufacturing (±5% deviation, Q>20).

4. Capacitors
   Use temperature compensation type capacitors. LAPIS recommends capacitors with CH characteristics.
   LAPIS recommends low-dielectric capacitors (class I) of 0±60 ppm/°C or less for areas that affect radio communication characteristics.

5. Resistors
   Use resistors which have small resistance to the temperature change.

Revision History

Document No.	Issue date	Page		NOTE
		Before	After	
FEXL7105DG-01	2013.04.25	–	–	Final 1st edition
FEXL7105DG-02	2014.12.8	Cover 6 10	Cover 6 10	Changed LAPIS logotype Added damping resistor at 32.768kHz external input mode Delete about the Low power clock built-in crystal oscillator input circuit Figure 5.1 Modified instances name